CLAIMS

What is claimed is:

1. A semiconductor package, comprising:

a substrate unit having an upper surface, a lower surface, a side surface connecting the upper surface and the lower surface, a plurality of circuit traces formed on the upper surface, a plurality of recessions formed on the side surface and electrically connecting to the circuit traces, and a metal layer formed on each of the recessions; and

a chip having an active surface and a back surface, wherein a plurality of bonding pads are formed on the active surface, a plurality of bumps formed on the bonding pads and the active surface of the chip faces to the upper surface of the substrate and is electrically connected to the substrate via the bumps.

2. The semiconductor package of claim 1, wherein the metal layer comprises a copper layer, a nickel layer and a gold layer.

3. The semiconductor package of claim 1, further comprising an underfill filled between the upper surface of the substrate unit and the active surface of the chip.

4. The semiconductor package of claim 1, wherein the substrate unit further comprises a plurality of electrically connecting devices on the metal layer.

5. The semiconductor package of claim 4, wherein the electrically connecting devices are solder balls.

6. A semiconductor package, comprising:

a substrate unit having an upper surface, a lower surface, a side surface connecting the upper surface and the lower surface, a plurality of circuit traces

formed on the upper surface, and a plurality of contacts formed on the side surface and electrically connecting to the circuit traces; and

a chip having an active surface and a back surface, and disposed on the upper surface of the substrate and electrically connected to the substrate.

7. The semiconductor package of claim 6, further comprising an underfill filled between the upper surface of the substrate unit and the active surface of the chip.

8. The semiconductor package of claim 6, wherein the substrate unit further comprises a plurality of electrically connecting devices formed on the contacts.

9. A semiconductor package module, comprising:

a first substrate unit having a first upper surface, a first lower surface, a first side surface connecting the first upper surface and the first lower surface, a plurality of first circuit traces formed on the first upper surface, and a plurality of first contacts formed on the first side surface and electrically connecting to the first circuit traces;

a first chip having a first active surface and a first back surface, and disposed on the first upper surface of the first substrate unit and electrically connected to the first substrate unit;

a second substrate unit having a second upper surface, a second lower surface, a second side surface connecting the second upper surface and the second lower surface, a plurality of second circuit traces formed on the second upper surface, and a plurality of second contacts formed on the second side surface and electrically connecting to the second circuit traces;

a second chip having a second active surface and a second back surface, and disposed on the second upper surface of the second substrate unit and

electrically connected to the second substrate unit;

a plurality of first electrically conductive devices formed on the first contacts; and

a plurality of second electrically conductive devices formed on the second contacts.

10. The semiconductor package module of claim 9, further comprising an adhesive disposed between the first lower surface of the first substrate unit and the second back surface of the second chip so as to attach the first lower surface of the first substrate unit to the second back surface of the second chip.

11. The semiconductor package module of claim 9, further comprising a module substrate electrically connecting the first substrate unit and the second substrate unit via the first electrically connecting devices and the second electrically connecting devices.

12. The semiconductor package module of claim 9, further comprising an underfill filled between the first upper surface of the first substrate unit and the first active surface of the first chip.

13. The semiconductor package module of claim 9, further comprising an underfill filled between the second upper surface of the second substrate unit and the second active surface of the second chip.

14. A substrate unit adapted to a semiconductor package, comprising:

an upper surface;

a lower surface opposed to the upper surface;

a side surface connecting the upper surface and the lower surface;

a plurality of circuit traces formed on the upper surface;

a plurality of recessions formed on the side surface and electrically connected to the circuit traces; and

a metal layer formed on one of the recessions.

15. The substrate unit of claim 14, wherein the metal layer comprises a copper layer, a nickel layer and a gold layer.

16. A substrate unit adapted to a semiconductor package, comprising:

an upper surface;

a lower surface opposed to the upper surface;

a side surface connecting the upper surface and the lower surface;

a plurality of circuit traces formed on the upper surface; and

a plurality of contacts formed on the side surface and electrically connected to the circuit traces.

17. A semiconductor package manufacturing method, comprising:

providing a chip, the chip having an active surface, a back surface, a plurality of bonding pads formed on the active surface and a plurality of bumps formed on the bonding pads;

providing a substrate array having an upper surface, a lower surface, a cutting street formed on the upper surface, and a plurality of through holes formed at the cutting street and passing through the upper surface and the lower surface, wherein the substrate array includes two substrate units separating from each other by the cutting street;

singualting the substrate array into two individual substrate units along the

cutting street to form a plurality of recessions on the individual substrate units;

disposing the chip on the individual substrate unit and electrically connected to the individual substrate unit via a plurality of bumps; and

forming a plurality of electrically connecting devices on the recessions.

18. The semiconductor package manufacturing method of claim 17, wherein each through hole has an inner wall, and a metal layer is formed on the inner wall.